

## Introduction

The ISL6539 is capable of providing a complete solution for two independent switching regulators. The ISL6539 can be configured to operate as a dual switching regulator or as a DDR regulator. This application note will focus on the ISL6539 configured as a dual switching regulator. For information on the ISL6539 configured as a DDR regulator, refer to either the datasheet[1] or to application note AN1279.

As a dual regulator, the ISL6539 provides control and protection for two independent rails. The switching frequency is fixed at 300kHz for both regulators. The two channels can be phase shifted 180° in order to minimize interaction. The ISL6539 incorporates voltage-feed-forward ramp modulation, current mode control, and internal feedback compensation which provides fast response to input voltage and output load transients. A PGOOD signal also is provided for both channels.

Protection features include under-voltage and over-voltage protection as well as a programmable over-current protection feature that utilizes the  $r_{DS(ON)}$  of the lower MOSFET. A more complete description of the ISL6539 can be found in the datasheet.

## Quick Start Evaluation

The ISL6539EVAL2 board is shipped 'ready to use' right from the box. The box includes this application note, the ISL6539 datasheet, and the evaluation board.

The evaluation board supports testing with laboratory power supplies. Both regulated outputs can be exercised through external loads. There are posts available on the two regulated output rails for drawing a load and/or monitoring the voltages. Two LEDs indicates the status of the individual channel PGOOD signals. There are also four scope probe points that allow for in depth analysis. Four jumpers have also been provided for control and monitoring purposes.

## Recommended Test Equipment

To test the full functionality of the ISL6539, the following equipment is recommended:

- Two laboratory power supplies
- Two Electronic Loads
- Four-channel Oscilloscope with probes
- Precision Digital Multimeters

## CIRCUIT SET UP

Refer to Figure 1 for locations of the jumpers, connectors and components described in the following sections.

## JUMPER SETTINGS

There are four jumpers on the board. Jumper JP1 is used to either enable or disable input voltage feed forward compensation. Jumper JP2 can be used to monitor the ISL6539 bias current by connecting an ammeter to the two jumper pins. If the bias current is not being monitored, this jumper must be shunted. Shunting jumper JP5 pulls the EN1 pin to VCC and is used to enable Channel 1. Shunting jumper JP6 enables Channel 2. Jumper J7 can be used to short the input rails of the two switching regulator channels. Table 1 provides a detailed description of the jumper descriptions and positions.

JUMPER	POSITION	FUNCTION
JP1	Toward VINPRG*	This will tie VIN pin to the input voltage for feed forward compensation.
	Away from VINPRG	This will tie VIN pin to GND, disabling input voltage feed forward compensation.
JP2	Shunted*	An ammeter may be connected across these pins to measure IC and GATE Drive current
JP5	Shunted*	CH1 enabled
	Removed	CH1 disabled
JP6	Shunted*	CH2 enabled
	Removed	CH2 disabled
JP7	Shunted*	The input rails for Channel 1 and Channel 2 are unified
	Removed	The input rails for Channel 1 and Channel 2 are independent
* Denotes default configuration		

**TABLE 1. DETAILED DESCRIPTION OF THE JUMPER SETTINGS**

## CONNECTING LOADS

Both regulated output rails are capable of both sourcing load current and sinking load current. Follow the directions below for the proper method of loading each rail.

*Loading VOUT1 - Sourcing Current:* This is the output rail of the Channel 1 regulator. Connect the positive terminal of an electronic load to the VOUT1 post (J5). Connect the return terminal of the same load to the adjacent GND post (J8).

*Loading VOUT1 - Sinking Current:* To test this channel while the regulator sinks current, connect the positive terminal of an electronic load to the VIN1 post (J3). Connect the return terminal of the same load to the VOUT1 post (J5).

**CAUTION:** *The return terminal of the load must float for this to work properly.*

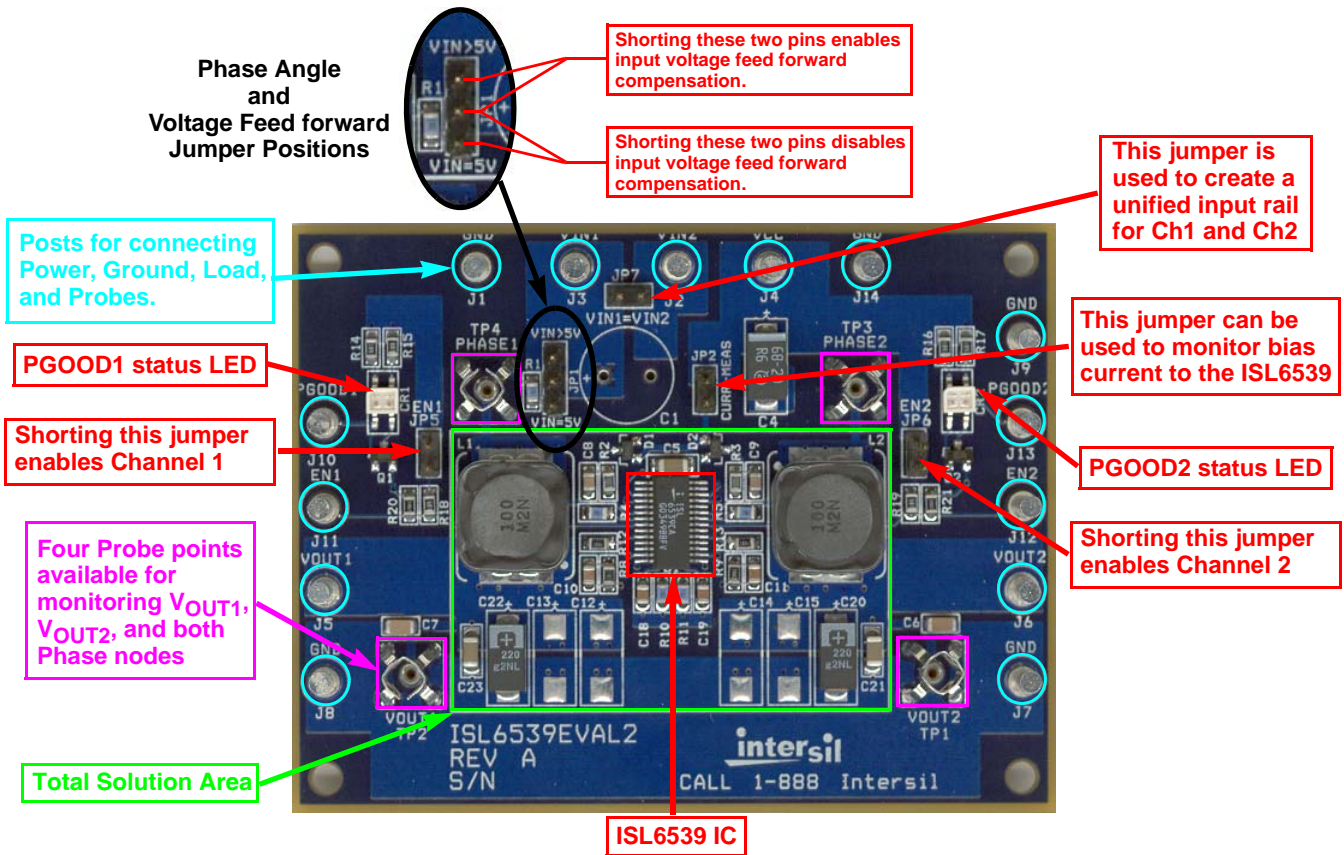


FIGURE 1. ISL6539EVAL1 BOARD

**Loading VOUT2 - Sourcing Current:** This is the output rail of the Channel 1 regulator. Connect the positive terminal of an electronic load to the VOUT2 post (J6). Connect the return terminal of the same load to the adjacent GND post (J7).

**Loading VOUT2 - Sinking Current:** To test this channel while the regulator sinks current, connect the positive terminal of an electronic load to the VIN2 post (J2). Connect the return terminal of the same load to the VOUT2 post (J6).

**CAUTION:** The return terminal of the load must float for this to work properly.

**CONNECTING PROBES**

Table 2 lists all the locations available for monitoring. The scope probe test points provide a low impedance ground connection and all GND posts can be utilized as a ground connection for probes.

TYPE	VOLTAGE	LOCATION
POST	VOUT1	J5
	VOUT2	J6
	VPGOOD1	J10
	VPGOOD2	J13
	VCC	J4
	VEN1	J11
	VEN2	J12
	VIN1	J3
	VIN2	J2
SCOPE PROBE TEST POINT	GND	J1, J7, J8, J9, J14
	VOUT1	TP2
	VOUT2	TP1
	VPHASE1	TP4
	VPHASE2	TP3

TABLE 2. PROBE TYPES AND LOCATIONS

## CONNECTING POWER

Prior to connecting the power supplies to the evaluation board, the power supplies should either be turned off or the outputs should be disabled.

**VCC Power Connection:** Connect the positive terminal of a laboratory power supply to the VCC post (J4). Connect the return terminal of the same load to the adjacent GND post (J14). The VCC voltage should be 5V.

**VIN1 Power Connection:** Connect the positive terminal of a laboratory power supply to the VIN1 post (J3). Connect the return terminal of the same load to the adjacent GND post (J1). This supply can be set from a minimum of  $1.2 \cdot V_{OUT1}$  to a maximum of 18V.

**VIN2 Power Connection:** Connect the positive terminal of a laboratory power supply to the VIN2 post (J2). Connect the return terminal of the same load to the adjacent GND post (J14). This supply can be set from a minimum of  $1.2 \cdot V_{OUT2}$  to a maximum of 18V.

If Jumper JP7 is shorted, then only apply voltage at one of the input voltage posts. It should be noted that a single 5V supply can be used to apply power to all three of these rails simultaneously.

## Operation

### ENABLING REGULATORS

The two switching regulators can be enabled by simply shorting jumpers J5 and J6 to enable Channels 1 and 2, respectively. Alternatively, with the jumpers left open, an external signal generator can be used to enable either channel through the EN1 post (J11) or the EN2 post (J12).

### APPLY POWER

The VIN power supplies must be turned on or enabled prior to turning on or enabling the VCC power supply. Likewise, they must always be disabled or turned off after disabling or turning of the VCC power supply. This rule does not apply if the VIN rails are to be supplied via the same power supply that is providing VCC.

The PGOOD status LEDs will give a visual indication of the  $V_{OUT1}$  and  $V_{OUT2}$  regulator levels. Table 3 describes the two states of the LEDs.

LED	CONDITION	RESULT
CR1	Green	$V_{OUT1}$ WITHIN PGOOD RANGE
	Red	$V_{OUT1}$ OUTSIDE PGOOD RANGE
CR1	Green	$V_{OUT2}$ WITHIN PGOOD RANGE
	Red	$V_{OUT1}$ OUTSIDE PGOOD RANGE

TABLE 3. PGOOD STATUS LED CONDITION INDICATOR

## EXAMINE WAVEFORMS

Start up is immediate following Power On Reset (POR). Using an oscilloscope or other laboratory equipment, the ramp-up and/or regulation of the outputs and other aspects of the regulator operations can be studied. Loading of the outputs can be accomplished through the use of electronic loads. Any other method, however, will work as well.

## Evaluation Board Design

### General

The evaluation board is built on a 2-ounce, four layer printed circuit board. The board is designed to support a continuous load of 5A on both regulated output rails while operating at room temperature and under natural convection cooling.

The schematic, bill of material, and the layout plots for the ISL6539EVAL1 evaluation board on provided at the end of this application note.

## Eval Board Performance

### Power Up

When the VCC voltage exceeds the POR level, the ISL6539 will begin the soft-start procedure. Figure 2 shows the startup of both regulated rails from POR.

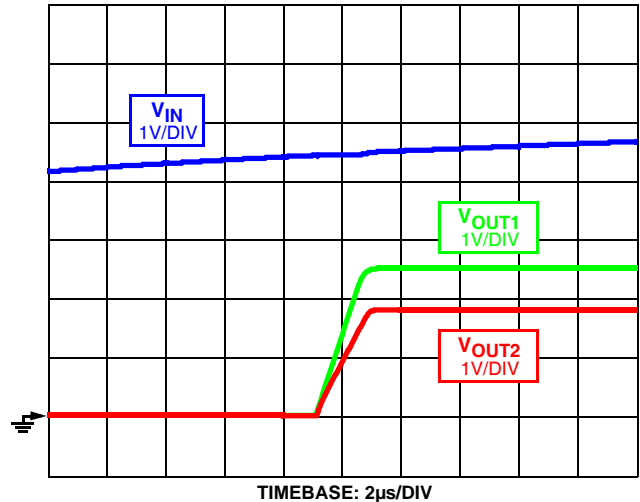


FIGURE 2. POR SOFT-START,  $V_{IN1} = V_{IN2} = V_{CC}$

Figure 3 shows the start up of both regulators via their respective enable inputs. Figure 3 also shows how the ISL6539 is capable of starting into a prebiased output rail. The  $V_{OUT1}$  rail has a 1V prebias prior to the enable being pulled high.

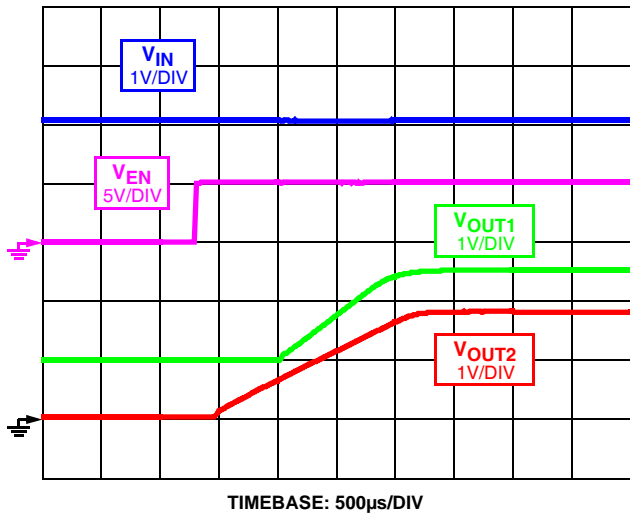


FIGURE 3. ENABLED SOFT-START,  $V_{IN1} = V_{IN2} = V_{CC}$

**Output Ripple**

Figure 4 shows the ripple on both the regulator outputs. This capture illustrates the 180° phase shift between the two regulators.

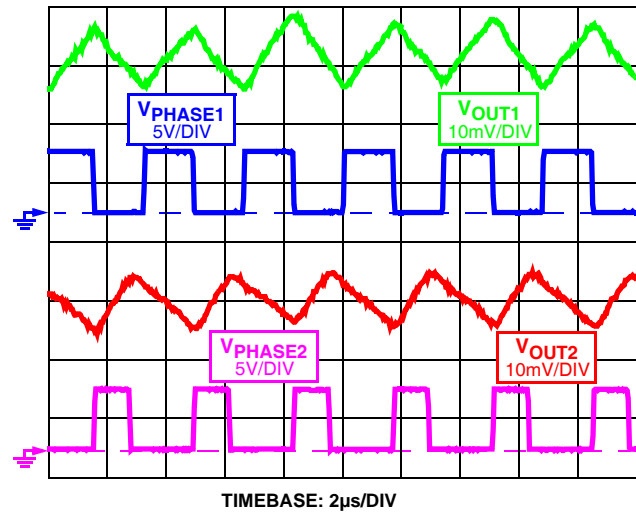


FIGURE 4. OUTPUT RIPPLE - 90° PHASE SHIFT,  $V_{IN1} = V_{IN2}$

**Transient Performance**

Figure 5 shows the response of the regulators while each is being stressed by a separate transient load. This instance is shown with a unified input rail.

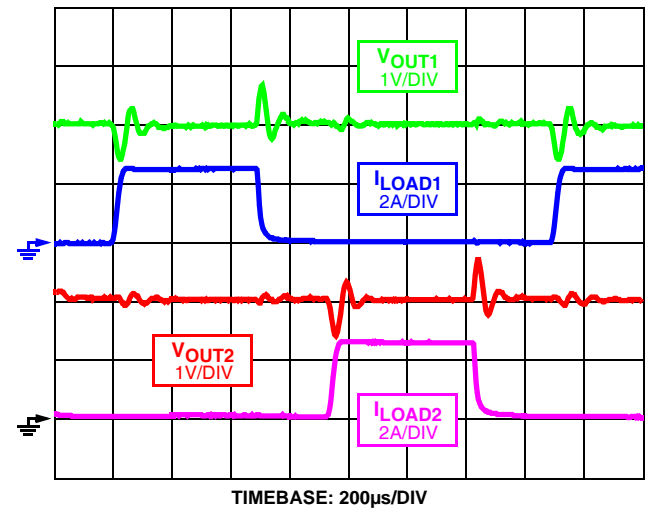


FIGURE 5. TRANSIENT LOAD ON  $V_{OUT1}$  AND  $V_{OUT2}$ ,  $V_{IN1} = V_{IN2}$

**Efficiency**

Figure 6 shows the efficiency of the individual regulators. These efficiencies were measured while the complementary regulator was disabled. The power dissipation of the ISL6539 is not included in the efficiency curves.

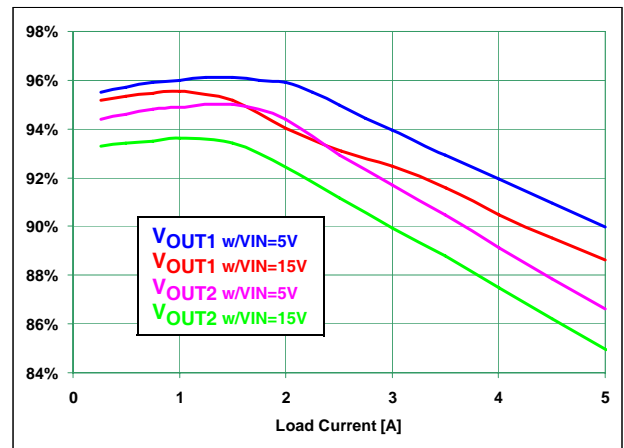


FIGURE 6. EFFICIENCY

### **ISL6539EVAL2 Customization**

There are numerous ways in which a designer might modify the ISL6539EVAL2 evaluation board for differing requirements. Some of the changes which are possible include:

- The output inductors, L1 and L2, for the  $V_{OUT1}$  and  $V_{OUT2}$  regulators, respectively.
- The input capacitance may be changed. The evaluation board is shipped with two 10 $\mu$ F ceramic capacitors, C2 and C3, as the input capacitance. A spot has been set aside for the installation of a 10mm diameter through hole aluminum electrolytic capacitor in location C1.
- The output capacitance of either regulator may be modified. The evaluation board is shipped with one 220 $\mu$ F capacitor on the output of each regulator. There are two empty locations, C12 and C13, available for the  $V_{OUT1}$  regulator and two empty locations, C14 and C15, available for the  $V_{OUT2}$  regulator.
- The overcurrent trip point of both the  $V_{OUT1}$  and  $V_{OUT2}$  regulators, programmed through the OCSET resistors, R10 and R11, respectively. Refer to the ISL6539 datasheet for details on this.
- Changing the value of C18 and C19 will alter the rise time of the outputs during soft-start. Refer to the ISL6539 datasheet for details on this.
- The load capacity for either rail can be increased by exchanging the MOSFETs, U2 and U3, for ones with higher current handling capabilities. The ISEN resistor values, R4 and R5, may need to be modified if this is done. The overcurrent resistor values, R10 and R11, would also have to be reviewed. Refer to the ISL6539 datasheet for details on calculating the values of these resistors.
- The output voltage of the  $V_{OUT1}$  regulator may be modified by changing resistor R12 and the output voltage of  $V_{OUT2}$  may be modified by changing resistor R13. Refer to the ISL6539 datasheet for details on this.

### **Conclusion**

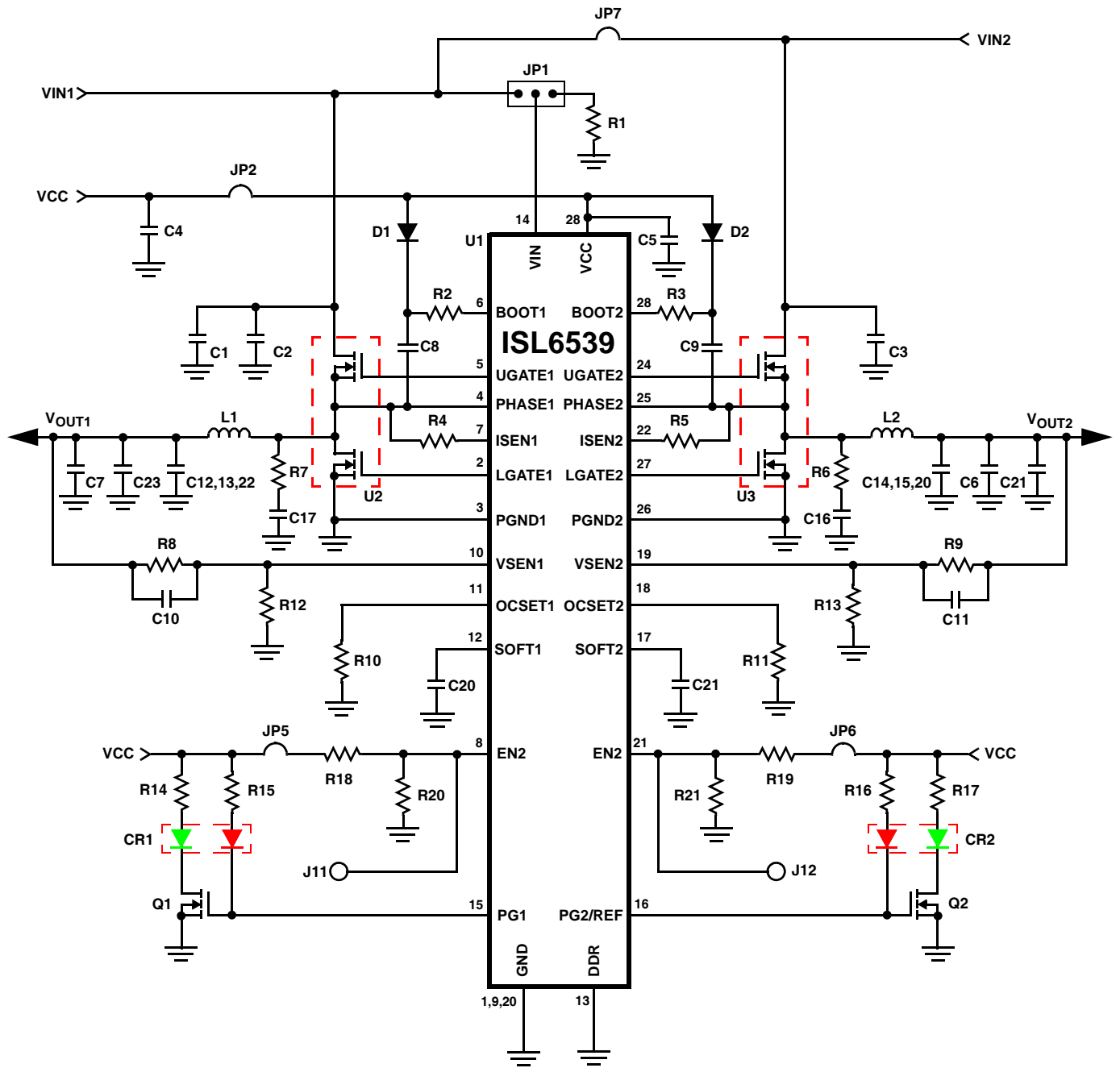
The ISL6539EVAL2 is a versatile platform that allows designers to gain a full understanding of the functionality of the ISL6539 when serving as a dual voltage regulator. The board is also flexible enough to allow the designer to modify the board for differing requirements. The following pages provide a schematic, bill of materials, and layout drawings to support implementation of this solution.

### **References**

For Intersil documents available on the web, see <http://www.intersil.com/>

- [1] *ISL6539 Data Sheet*, Intersil Corporation, File No. FN9144.

ISL6539EVAL2 Schematic



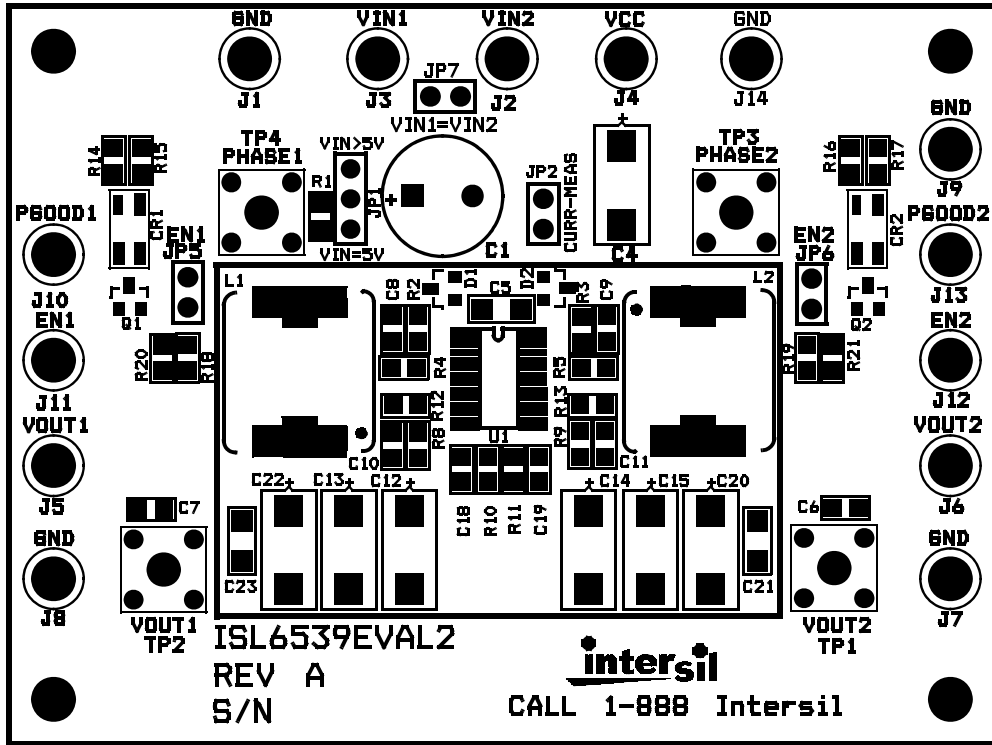
## Application Note 1279

### ISL6539EVAL2 Bill of Materials (BOM)

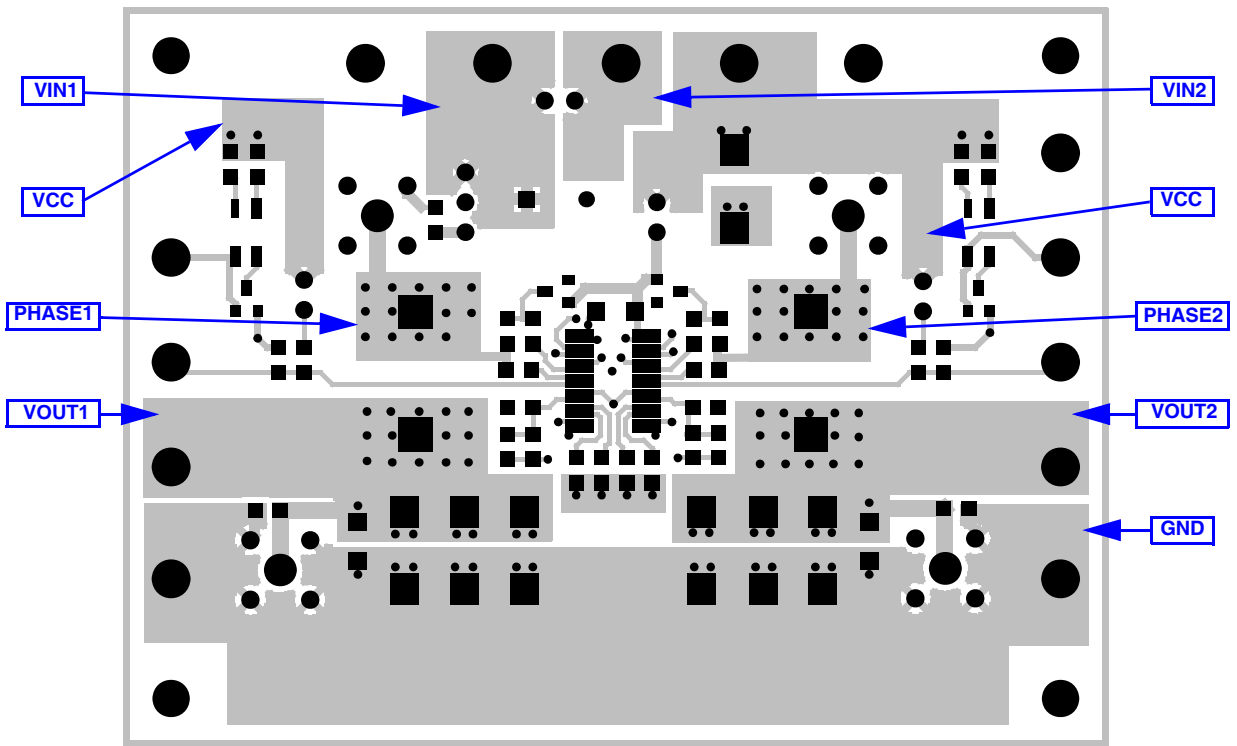
QTY	REFERENCE	DESCRIPTION	VENDOR	MFG. PART NO.
2	C2, C3	CAPACITOR, SMD, 1812, 10µF, 25V, 20%, X5R	TAIYO YUDEN	TMK432BJ106MM
1	C4	CAPACITOR TANT, LOW ESR, SMD, D, 68µF, 16V, 10%	KEMET	T494D686K016AS
3	C5, C21, C23	CAPACITOR, SMD, 1206, 4.7µF, 10V, 10%, X7R	VENKEL	C1206X7R100475KNE
2	C6, C7	CAPACITOR, SMD, 1206, 1µF, 10V, 10%, X7R	KEMET	C1206C105K8RAC
2	C8, C9	CAPACITOR, SMD, 0805, 0.15µF, 25V, 10%, X7R	PANASONIC	ECJ-2YB1E154K
4	C10, C11, C18, C19	CAPACITOR, SMD, 0805, 0.01µF, 50V, 10%, X7R	PANASONIC	ECJ-2VB1H103K
2	C20, C22	CAPACITOR TANT, LOW ESR, SMD, D2, 220µF, 4V, 20%	SANYO	4TPC220M
2	CR1, CR2	LED, SMD, 3x2.5mm, 4P, RED/GRN, 12/20MCD, 2V	LUMEX	SSL-LXA3025IGC-TR
2	D1, D2	DIODE-SCHOTTKY, SMD, SOT323, 3P, 30V, 0.2A	ON-SEMICONDUCTOR	BAT54WT1-T
2	L1, L2	COIL-PWR INDUCTOR, SMD, 12mm, 4.7µH, 20%, 5.7	SUMIDA	CDRH124-4R7MC
2	Q1, Q2	TRANSISTOR, N-CHANNEL, 3P, SOT23, 100V, 0.17A	ON-SEMICONDUCTOR	BSS123LT1-T
3	R1, R10, R11	RESISTOR, SMD, 0805, 100k, 1/10W, 1%, TF	PANASONIC	ERJ-6ENF1003V
2	R2, R3	RESISTOR, SMD, 0805, 0Ω, 1/10W, TF	PANASONIC	ERJ-6GEY0R00V
2	R4, R5	RESISTOR, SMD, 0805, 2k, 1/10W, 1%, TF	PANASONIC	ERJ-6ENF2001V
1	R8	RESISTOR, SMD, 0805, 17.8k, 1/10W, 1%, TF	PANASONIC	ERJ-6ENF1782V
5	R9, R12, R13, R20, R21	RESISTOR, SMD, 0805, 10k, 1/10W, 1%, TF	PANASONIC	ERJ-6ENF1002V
6	R14 - R19	RESISTOR, SMD, 0805, 680Ω, 1/10W, 5%, TF	PANASONIC	ERJ-6GEYJ681V
1	U1	IC, DUAL SWITCHER, 30V, 28PIN, QSOP, DDR OPTION	INTERSIL	ISL6539CA
2	U2, U3	MOSFET, DUAL, N-CHANNEL, LOGIC, 8P, SOIC, 30V, 6A	FAIRCHILD	FDS6912A



ISL6539EVAL2 Printed Circuit Board Layers



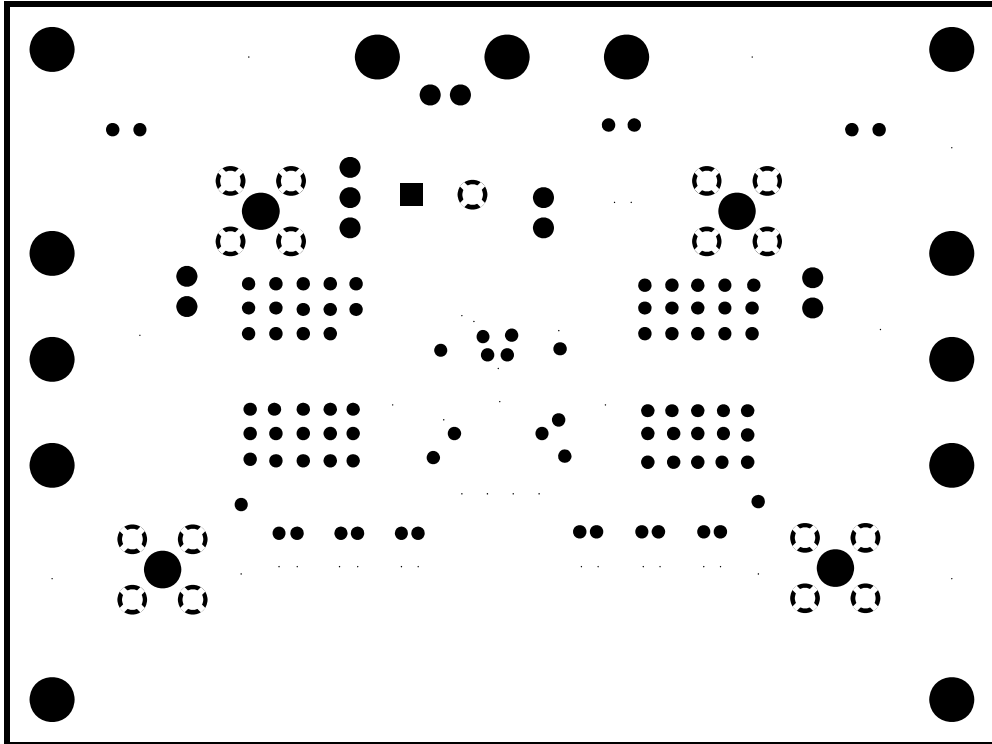
ISL6539EVAL2 - TOP SILK SCREEN AND SOLDERMASK



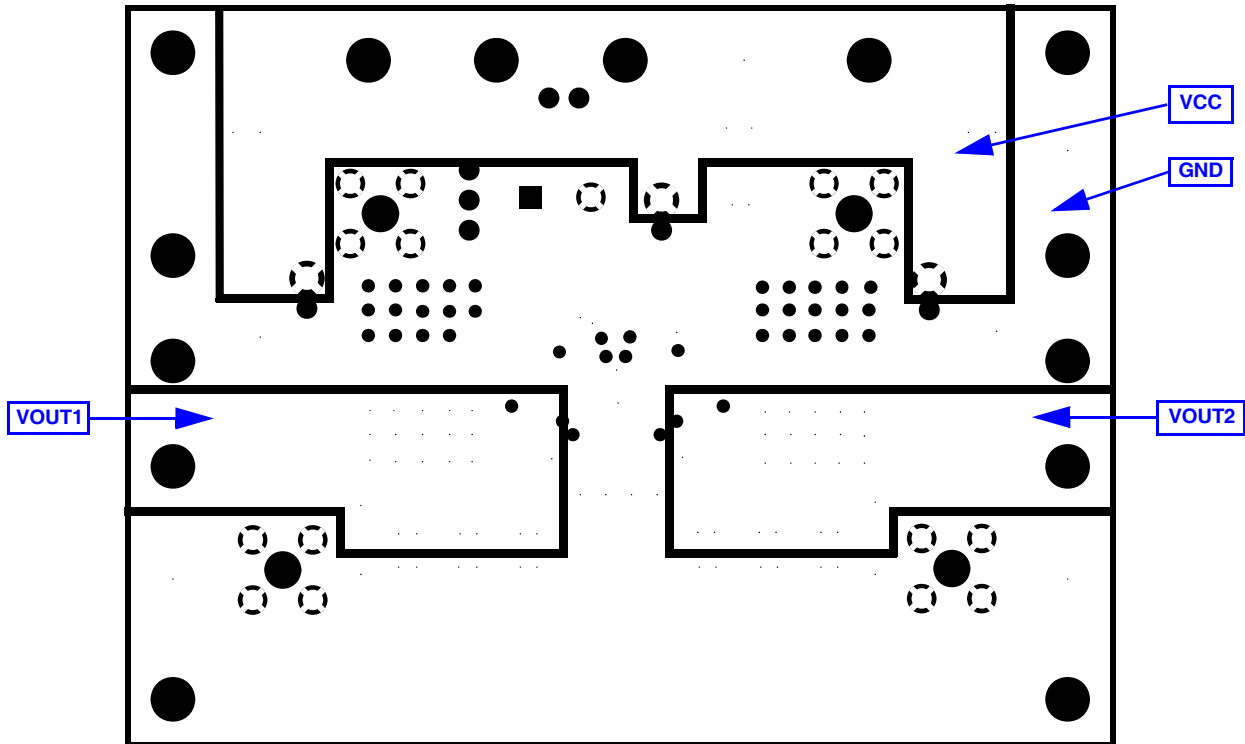
ISL6539EVAL2 - TOP COPPER LAYER



ISL6539EVAL2 Printed Circuit Board Layers (Continued)

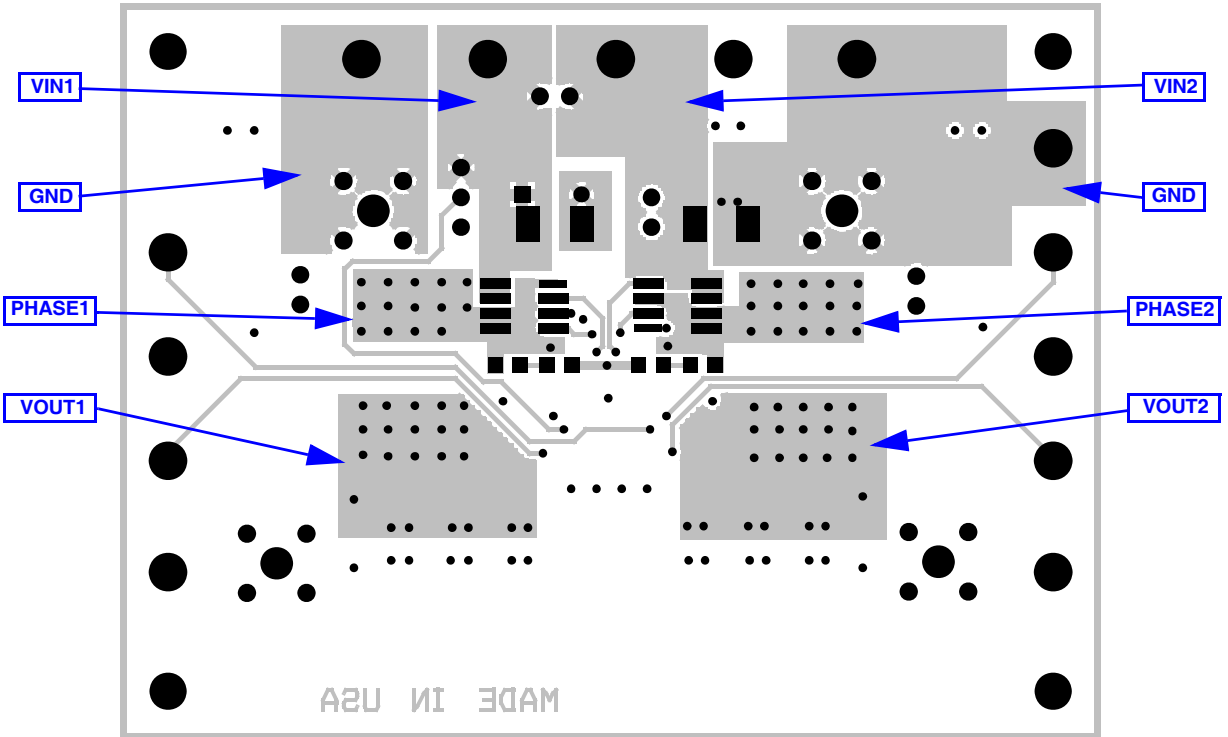


ISL6539EVAL2 - LAYER 2 - GROUND

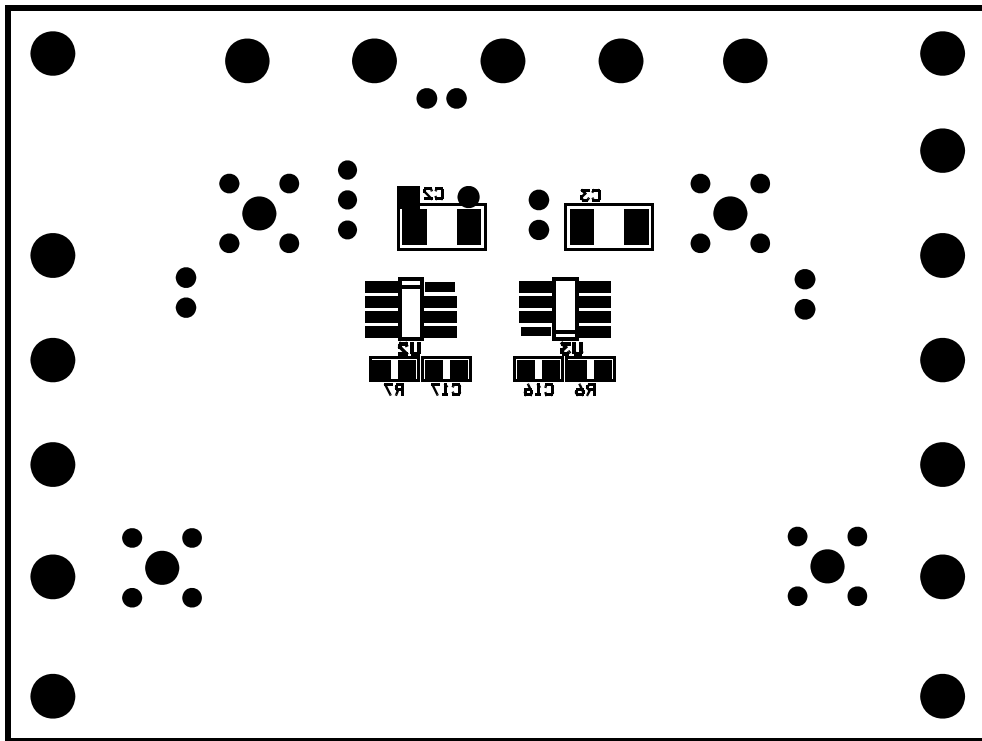


ISL6539EVAL2 - LAYER 3 - POWER

ISL6539EVAL2 Printed Circuit Board Layers (Continued)



ISL6539EVAL2 - BOTTOM LAYER



ISL6539EVAL2 - BOTTOM SILK SCREEN AND SOLDER MASK

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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